All-Optical Phase Control of a Square-Wave Photonic Clock

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***Abstract*—We propose and demonstrate an all-optical technique to control the phase of a class of square-wave photonic clocks. The particular photonic clock used for our demonstration is comprised of a traveling-wave semiconductor optical amplifier (SOA) connected to a resonant-type SOA exhibiting hysteresis. Phase control is achieved by cross-gain modulation within the travelling-wave (TW)-SOA, which suspends clock generation over a controlled time interval to achieve the desired phase. We used 1576-nm control pulses with 62-μW peak power and arbitrary polarization states, features that are telecommunications compatible. A useful feature of our scheme is that phase control is independent of the synchronization between the initial clock phase and arrival time of the control pulse.**

***Index Terms*—Clocks, flip-flops, optical bistability, optical signal processing.**

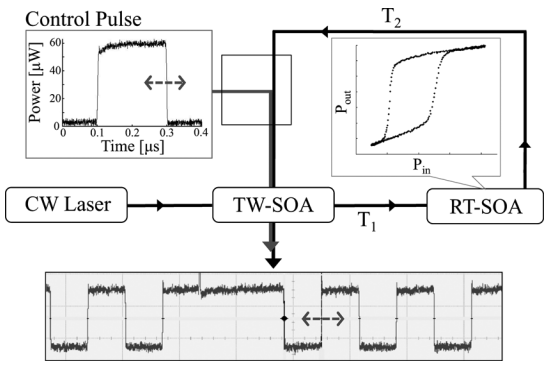

Fig. 1. Principle of operation for all-optical phase control. Left inset shows an example of a control pulse. Right inset shows the hysteresis of the bistable RT-SOA. Bottom graphic shows a clock signal whose phase is optically controlled. Dashed arrows illustrate that the timing of the control-pulse trailing edge controls the phase of the clock.

SQUARE-WAVE clock signals are an integral part of signal processing in the electrical domain [1], [2], providing well-defined ON/OFF states to drive functional electronic gates. Similarly, *optical* square-wave clock signals are expected to play an integral role in the advancement of signal processing in the *optical* domain [3], [4]. Two schemes have been demonstrated for optical square-wave signal generation based on the nonlinear response of semiconductor optical amplifiers (SOAs). One scheme uses a continuous-wave (CW) laser along with a Mach–Zehnder interferometer with integrated SOAs [3]. The other scheme uses a CW laser along with a bistable resonant-type SOA (RT-SOA) coupled to a travelling-wave SOA (TW-SOA) [4]. In each scheme, square-wave signal generation is realized by variations in the SOA carrier density produced by changes in optical power. In this sense, these schemes can be considered to be two examples of a general class of photonic clocks. Mode-locked lasers constitute another class of photonic clocks, and recent research aims to flatten the top of the initially sharp-peaked pulses from such sources [5].

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In each of the two SOA-based photonic-clock demonstrations, a clock signal was generated whose phase was not controlled externally. Instead, the clock phase was determined by the nonprecise process of powering on the CW laser and various SOAs, and adjusting the experimental power levels. This nonprecise process is embodied in the title of [3], which refers to its photonic clock as "self-starting."

In this letter, we describe the principle of operation of a technique used to realize "controlled start" of the clock signal, resulting in a clock phase that can be controlled by an external optical pulse. This pulse exhibits an optical power and wavelength range that is compatible with telecommunication systems, and phase control does not depend on the synchronization between the initial clock phase and the arrival time of the control pulse. We demonstrate this control technique for a specific photonic-clock scheme (initially demonstrated in [4]), but it is applicable to the whole class of SOA-based photonic clocks described above.

I. Principle of Operation

The principle of operation for phase control is shown in Fig. 1 along with the photonic clock scheme used in our experiments. The photonic clock works as follows. A CW signal from a diode laser is passed through a TW-SOA and then into a RT-SOA that exhibits the bistable input-output hysteresis curve shown in the figure's right-most inset. The optical output signal from the RT-SOA is fed back through the TW-SOA and then exits the clock system.

As the RT-SOA output signal passes through the TW-SOA, it operates on CW input signal by cross-gain modulation (XGM)

within the TW-SOA. When the RT-SOA bistable output power is on the upper hysteresis branch, relatively strong power saturates the TW-SOA gain. The associated XGM causes the input power to the RT-SOA to fall below the bistable region a time T_1 later. The bistable output power then falls to the lower hysteresis branch, and at a time T_2 later, this low-power optical signal reaches the TW-SOA, desaturating the gain and causing the input power to the RT-SOA to increase above the bistable region once again. A square-wave signal is generated as the optical power repeatedly varies above and below the bistable switching thresholds. The time taken to complete one cycle determines the clock period, i.e., $T_{\rm clk} \approx 2(T_1 + T_2)$.

All-optical phase control works as follows. We assume the availability of an optical control pulse with the desired phase information that is being distributed to a remote optical clock through a lightwave system. Such a pulse, whose wavelength falls within the TW-SOA gain spectrum, operates on the clock by XGM. This control pulse saturates the TW-SOA gain, forcing the input power to the RT-SOA to fall below the downward-switching threshold of the hysteresis curve and forcing the output power to the lower branch of the hysteresis. So long as the control pulse is present in the TW-SOA, the RT-SOA output power remains in this low state. At a time $(1/2)T_{\rm clk}$ after the trailing edge of the control pulse exits the TW-SOA, however, the TW-SOA gain recovers and the signal power into the RT-SOA rises above the upward-switching threshold and clock operation resumes. The phase of the resumed clock signal is thus determined by the timing of the trailing edge of the control pulse.

II. Experimental Setup

The experimental setup to demonstrate phase control over a self-starting photonic clock is shown in Fig. 2; components used to generate the control pulses are grouped by a dashed box, and paths through which signals are counter-propagating are drawn as double lines. The RT-SOA is a Fabry-Perot SOA (FP-SOA) biased at 67.5 mA (3.4 mA above lasing threshold) and the TW-SOA (CIP, SOA-XN-OEC-1550) is biased at 54.3 mA to provide approximately 8-dB gain. The clock laser is an external-cavity DFB laser set to a wavelength of 1590.654 nm. Two polarization controllers are used within the feedback path to align the polarization into the FP-SOA and TW-SOA; clock generation requires precise polarization alignment [4].

A circulator is located on either side of the TW-SOA to allow for the CW laser signal to propagate through the TW-SOA in a direction counter to the RT-SOA output and control pulse. Circulator 2 directs the RT-SOA output back through the TW-SOA. Circulator 1 sorts the TW-SOA output signal from the incoming CW input signal, directing the former to a 22-GHz bandwidth Discovery Semiconductors photodiode and 1-GHz oscilloscope for analysis. Bandpass filters having 3-dB bandwidths of 1 nm (at the RT-SOA output) and 3 nm are used to remove the broadband amplified spontaneous emission from the TW- and RT-SOA devices.

Optical control pulses are generated using a 1576-nm DFB diode laser, a Mach–Zehnder amplitude modulator, and an electrical pulse-pattern generator. These pulses have a period of 1 ms and rise and fall times of 3.2 and 3.3 ns, respectively. An

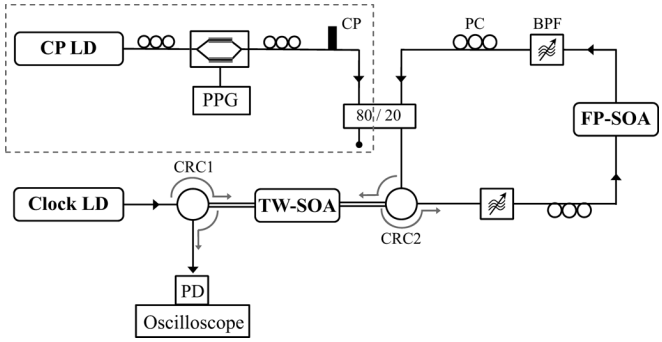

Fig. 2. Experimental setup for demonstration of phase control. The dashed box encloses components for control-pulse generation. CP: control pulse. LD: laser diode. PPG: pulse pattern generator. CRC: circulator. PC: polarization controller. BPF: bandpass filter. PD: photodiode.

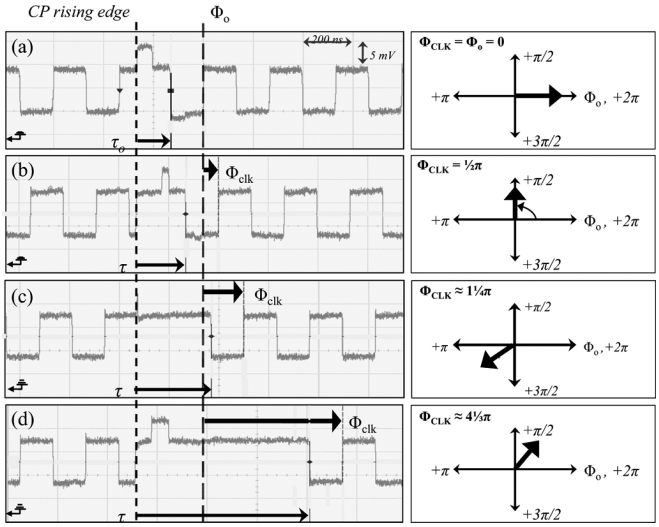

Fig. 3. All-optical phase control of a square-wave photonic clock. The left dashed line and the lower arrow highlight the beginning and duration of the control pulse, respectively, for each oscilloscope trace. The right dashed line marks the initial clock phase Φ_0 and the upper arrow marks the controlled change in phase for each trace. This change in phase is depicted at the right by phasor diagrams. (a) $\tau_0 = 134$ ns, establishing $\Phi_0 = 0$; (b) $\tau = 200$ ns, $\Phi_{\rm clk} = \pi/2$; (c) $\tau = 300$ ns, $\Phi_{\rm clk} \approx 5\pi/4$; (d) $\tau = 700$ ns, $\Phi_{\rm clk} \approx 4(1/3)\pi$. $(1/2)T_{\rm clk} = 132$ ns.

80/20 splitter couples the control pulse into the path of the clock signal; control pulses of 62-μW peak power are delivered to the TW-SOA after Circulator 2. A polarization controller is used before the 80/20 splitter to test the sensitivity of phase control to the control-pulse polarization.

III. Experimental Results

The experimental results are shown in Fig. 3 for four values of the control-pulse width τ and resulting clock phase $\Phi_{\rm clk}$ (see (1)); on the left are the oscilloscope traces of the clock output and on the right are the phasor diagrams. The oscilloscope traces show the clock output power and control-pulse power together, as a bandpass filter was not available for demultiplexing. The square-wave clock used for experiments exhibited a clock frequency of 3.78 MHz, corresponding to a half-period of 132.17 ns with a jitter of 0.58 ns.

To quantify phase control, we establish an initial phase, Φ_0, associated with the initial control-pulse duration τ_0. The clock

phase $\Phi_{\rm clk}$ is defined as the offset from Φ_0, and is determined by the control-pulse duration τ as follows:

$$\Phi_{\rm clk} = \frac{(\tau - \tau_0)}{0.5T_{\rm clk}}\pi. \quad (1)$$

Thus, by increasing the control-pulse width τ from its nominal value τ_0, any value of clock phase can be achieved. For an increase in τ that is a multiple of $T_{\rm clk}$, there is an additional delay of $m2\pi$ to the clock cycle where m is an integer.

Fig. 3(a) depicts the nominal clock phase Φ_0, using the nominal control-pulse width $\tau_0 = 134$ ns, which is slightly longer than $(1/2)T_{\rm clk}$. This time represents a minimum time delay for this phase-control scheme. We arbitrarily choose $\Phi_0 = 0$. Parts (b) – (d) show clock phase delays from this initial value, each for different durations of the control pulse width τ. In (b), $\tau = 200$ ns, corresponding to a phase delay of $(1/2)\pi$ according to (1). In (c), $\tau = 300$ ns for a resulting clock phase of a $5\pi/4$, and in (d) $\tau = 700$ ns, delaying the clock for greater than two full periods for a resulting clock phase of approximately $4(1/3)\pi$.

Examining the output in signals of Fig. 3, two important observations support that the phase is being controlled in a consistent, predictable manner. First, the time delay between the falling edge of the control pulse and the rising edge of the clock remains consistent. Over twenty acquisitions, ten each of $\tau = 200$ and 300 ns, the time from the falling edge of the control pulse to the rising edge of the resumed clock is 132.17 ns, equal to $1/2T_{\rm clk}$. The standard deviation of this measurement is 0.62 ns, equaling a clock-phase error of $0.62\,{\rm ns} \times 2\pi/Tclk = 14.8$ mrad, which is nearly the quadrature sum (0.61 ns, 14.5 mrad) of the clock jitter (0.58 ns, 13.8 mrad) and the control-pulse fall-time jitter (0.18 ns, 4.3 mrad).

Second, the clock resumes as expected independent of the synchronization between the control pulse arrival time and the initial clock phase. In part (a), for example, the rising edge of the control pulse coincides with the clock 'ON' level, while in parts (b) and (d), it coincides with the clock 'OFF' level. In part (c) the control pulse is coincident with a falling edge of the square-wave signal. In all cases, the clock resumes after a time delay of $(1/2)\mathrm{T}_{\rm clk}$ from the falling edge of the control pulse.

Phase control was consistently achieved independent of the control pulse polarization, with no measureable variation in amplitude or timing of the resumed clock signal. This polarization independence occurs because the power of the control pulse provides sufficient gain saturation to disable the clock in either the transverse-electric (TE) or transverse-magnetic (TM) modes of the TW-SOA.

The high optical-power ledge that appears within the duration of the control pulse in parts (a), (b), and (d) of Fig. 3 is an artifact of having both the control-pulse signal and clock output signal flow into the photodiode without spectrally demultiplexing them. (This ledge is narrow and appears as a spike in the clock signal shown at the bottom of the Fig. 1 schematic.) The ledge width is the duration over which the control pulse overlaps with the high output clock power. This ledge does not impact the resulting phase control.

The main applications of all-optical square-wave clocks are likely to be for data rates at 10 Gb/s and beyond, supporting optical signal processing of data. The all-optical clock used here is limited by the long fiber lengths of bulk components (~ 25 m per half clock period) to a fundamental frequency near 4 MHz [4]. We expect that this frequency can be increased by over three orders of magnitude by using photonic integration and by introducing feedback-path loops [3]. The phase-control technique demonstrated here is expected to keep pace with these clock-frequency enhancements since commercial TW-SOAs (e.g., CIP, SOA-XN-OEC-1550) currently exhibit gain-recovery times as low as 10 ps. Also, the *periodic* timing of the control pulses used in our experiments is not required for phase control; the general phase-control technique presented here is also applicable to *aperiodically* timed control signals.

IV. Conclusion

We propose and demonstrate all-optical phase control over a SOA-based square-wave photonic clock. Control is achieved by injection of an optical pulse that falls within the gain spectrum of the TW-SOA; varying the duration of this control pulse alters the phase of the clock independent of the synchronization between the control pulse and the initial clock signal. Control works at low optical power (< 0.1 mW) and for random polarization of the control pulse, making this technique suitable to a wide range of environments. Moreover, this control technique is applicable to a whole class of photonic clocks whose square-wave signal is generated by optical-power-induced variations in the SOA carrier density. We have considered the distribution of a known clock phase over a lightwave network; extraction of this phase from actual data signal remains as future research. Photonic clocks and their phase control may enable advanced sequential signal-processing applications in future photonic integrated circuits.

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