Optical Square-Wave Clock Generation Based on an All-Optical Flip-Flop

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***Abstract*—We demonstrate optical square-wave clock generation based on an all-optical flip-flop. The bistable output power from a resonant-type semiconductor optical amplifier (SOA) is switched ON and OFF by modulating its input with its output via cross-gain modulation in a traveling-wave SOA. All active components are driven by dc currents, and the wavelength and clock frequency are selectable. A clock frequency of 3.5 MHz is demonstrated, limited by the time of flight between bulk optical components. Optical square-wave clock signals are promising for applications in photonic integrated circuits and all-optical signal processing.**

***Index Terms*—Clocks, flip-flops, optical bistability, optical signal processing.**

I. Introduction

SQUARE-WAVE clock signals are an integral part of signal processing in the electrical domain [1], providing well-defined transitions between flat voltage plateaus that drive functional electronic gates. Similarly, realization of optical square-wave clock signals is expected to advance signal-processing capabilities in the optical domain, especially for photonic-integrated circuits. Mode-locking techniques are available to produce optical-clock signals, but such pulse trains do not exhibit flat power levels [2]. The flatness of mode-locked signals can be improved by temporal expansion and multiplication using specially designed fiber Bragg gratings, but experiments show pulse trains whose flat tops are of similar duration as their rise and fall times [3]. An optical clock signal has been successfully demonstrated using a Mach–Zehnder interferometer integrated with two internal semiconductor optical amplifiers (SOAs) [4].

In the electrical domain, clock signals are created by providing a feedback path between electrical flip-flops [1]. By analogy, an optical-clock signal should be realizable using an all-optical flip-flop, a device whose two-state, latchable optical output power can be controlled by set and reset optical signals [5]. Optical flip-flops have undergone intense research over the past decade for their potential utility in signal-processing applications, and come in many forms from waveguide geometries [6]–[8] to vertical-cavity designs [9], [10]. All of these demonstrated optical flip-flops are characterized by sharp transitions between the "ON" and "OFF" power levels; moreover, their nonlinear input–output transfer function exhibits flatter output levels than that of a Mach–Zehnder interferometer. We present the principle of operation for an optical-clock signal generated from an all-optical flip-flop, and demonstrate its performance at several wavelengths and clock frequencies. All active components used to generate the clock signal are driven with dc currents.

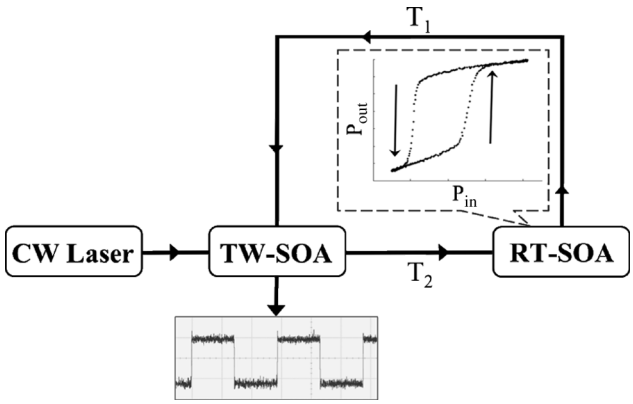

Fig. 1. General schematic for optical square-wave clock generation, using a TW-SOA and an RT-SOA. Inset shows the measured bistable hysteresis loop of the RT-SOA; arrows show direction of hysteresis loop.

II. Principle of Operation

The principle of operation for optical-clock generation is shown in Fig. 1. The continuous-wave (CW) light from a diode laser is passed through a traveling-wave SOA (TW-SOA) and then to a resonant-type SOA (RT-SOA). The optical output of the RT-SOA is then fed back to the TW-SOA through a feedback path.

The RT-SOA exhibits the bistable transfer function shown as the inset in Fig. 1. The square-wave optical clock is generated by sequentially bringing the optical power above the upward-switching threshold of the hysteresis and then below the downward-switching threshold. Suppose that the output power of the RT-SOA initially lies on the lower output branch

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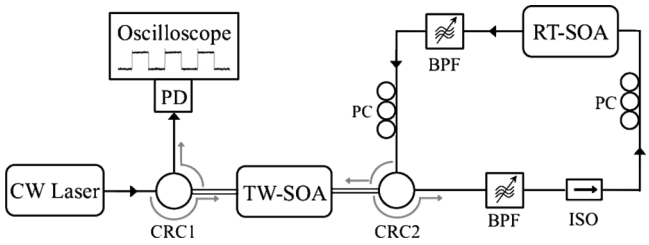

Fig. 2. Experimental setup. CRC = circulator; BPF = bandpass filter; ISO = isolator; PC = polarization controller; and PD = photodiode.

of the hysteresis loop with an input power below the upward-switching threshold. An increase of the input power (via increasing the CW laser output power, for example) beyond the upward-switching threshold causes the RT-SOA output power to switch to the upper output branch of the hysteresis loop, creating a sharp increase in output power.

After a time T_1, this sharp increase in power reaches the TW-SOA via the feedback path, and its amplification saturates the TW-SOA gain. Cross-gain modulation (XGM) then causes a decrease in the CW signal power that is being amplified simultaneously by the TW-SOA. After a time T_2, this reduced-power optical signal reaches the RT-SOA with an input power that falls below the downward-switching threshold of the hysteresis loop. The output power from the RT-SOA then falls from the upper to lower output branch.

After a time T_1, this decrease in power reaches the TW-SOA via the feedback path and allows the gain of the TW-SOA to recover from its more strongly saturated state. The resulting increase in the TW-SOA gain allows the CW signal to be amplified to its former extent, and the increased-power optical signal reaches the RT-SOA with an input power that once again exceeds the upward-switching threshold of the hysteresis loop. These actions comprise one cycle of the square-wave clock. The time taken to complete this cycle is approximately the period of the square wave generated: $T \approx 2(T_1 + T_2)$. Note that although the output square-wave signal is a function of time, all active components—the CW diode laser, the TW-SOA, and the RT-SOA—are driven by dc currents.

III. Experimental Setup

The experimental setup used to demonstrate all-optical clock generation is shown in Fig. 2; paths through which two signals are counterpropagating are drawn with double lines. The RT-SOA used is a Fabry–Pérot SOA (FP-SOA) biased at 67.5 mA (3.4 mA above lasing threshold) and the TW-SOA is biased at 54.3 mA to provide about 8 dB of gain. The CW laser is an external-cavity DFB laser set at an output power of 29 μW and a wavelength of 1590.654 nm, detuned by 0.04 nm to the long-wavelength side of the nearest longitudinal mode of the FP-SOA.

A circulator is located on each side of the TW-SOA to allow for the CW-laser signal and RT-SOA output to counterpropagate and interact with the TW-SOA gain. Circulator 2 directs the RT-SOA output back through the TW-SOA. Circulator 1 then sorts the TW-SOA output from the incoming CW input, directing it to a 1-GHz oscilloscope for analysis. The photodiode is a Discovery photodiode with a 22-GHz bandwidth. In

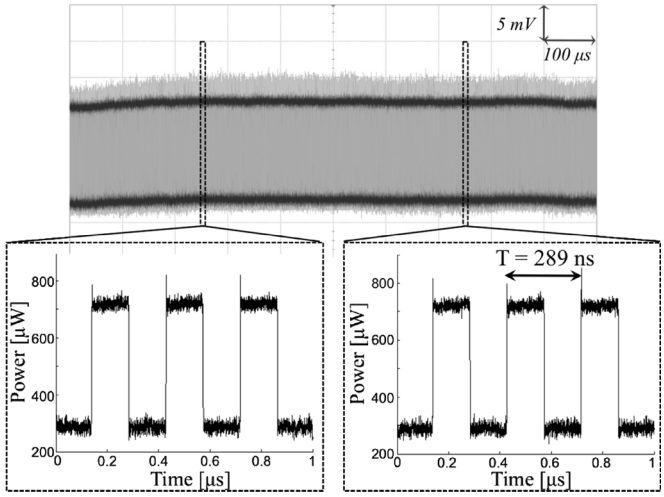

Fig. 3. Optical square-wave clock signal over a duration of 1 ms, consisting of 3460 cycles. Insets display details of the square-wave regions over 1-μs windows of the optical clock.

principle, the square-wave clock signal exists before and after the RT-SOA; for convenience, we chose to measure it after the TW-SOA, which amplifies the clock signal. Bandpass filters having 3-dB bandwidths of 1 nm (at the RT-SOA output) and 3 nm are used to remove the broadband amplified spontaneous emission from the TW- and RT-SOA devices, and an isolator ensures unidirectional, single-pass propagation through the system.

IV. Experimental Results

An optical square-wave clock signal generated by the setup in Fig. 2 is shown in Fig. 3 over a span of 1 ms; the insets show two 1-μs windows. This signal is characterized by a wavelength of 1590.654 nm, a clock frequency of 3.46 MHz, a rise time of 560 ps, a fall time of 740 ps, and an ON–OFF contrast of 4.4 dB. The bistable hysteresis arises in FP-SOAs from the tuning of FP resonances in response to gain saturation and the accompanying change in refractive index attributed to the free-carrier density [11]. The spike in power at the rising edge of the square wave is the result of a resonance peak of the FP-SOA passing the input signal wavelength during the switch from the lower to upper branch of the hysteresis [12]. This spike as well as high-frequency noise can be removed by passing the clock signal through a filter of suitable bandwidth.

The amplitude and contrast of the clock are highly sensitive to polarization fluctuations; such fluctuations alter the optical power injected into the active waveguide regions. The polarization controllers shown in Fig. 3 were required to optimize coupling of the signal into the active waveguide devices and to produce the stable clock pattern shown in Fig. 3. Monolithic integration of devices into a photonic integrated circuit is expected to stabilize polarization and clock operation.

Optical square-waves can be generated using the setup shown in Fig. 2 for a range of wavelengths and clock frequencies. Fig. 4(a) shows the longitudinal modes of the FP-SOA over a 1.5-nm span; the vertical lines mark the wavelength of the CW-laser signal λ_b, λ_c, and λ_d, used for generating the clock signals shown in parts (b)–(d). Each CW-signal wavelength lies

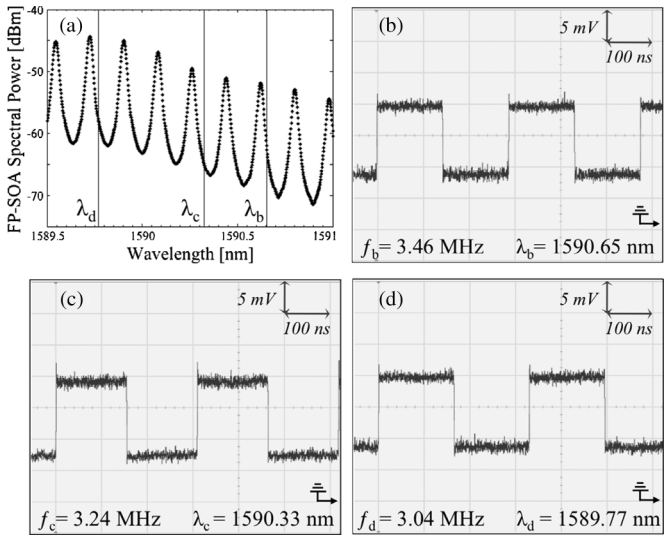

Fig. 4. Demonstration of selectable wavelength and clock frequency of the optical square-wave clock: (a) resonant modes of the FP-SOA, (b)–(d) clock signals for different holding beam wavelengths and clock frequencies.

on the long-wavelength side of the FP resonance with which it interacts to produce a bistable hysteresis of the same S-shape depicted in Fig. 1. FP resonances of sufficient strength to support bistability span a wavelength range of 40 nm for a given FP-SOA. Such a broad wavelength range of operation is important to adapt a single optical clock to the range of wavelength channels within a wavelength-division-multiplexed system. Moreover, within this wavelength range, the temperature of the FP-SOA can be used to provide fine wavelength-tuning of the resonances.

In addition to changing the wavelength, the clock frequency (i.e., the repetition rate) has also been varied in the examples shown in parts (b)–(d) of Fig. 4. In our experiment, the clock frequency was changed from 3.46 MHz in part (b) to lower values in parts (c) and (d) by adding fiber delay lines between the two SOA devices. Fiber lengths of (c) 2 m (d) and 4 m, increased the clock period by 20 and 40 ns, respectively. The maximum clock frequency in our experiment is limited by the length of the fibers in between the TW-SOA and the RT-SOA. Achieving higher clock frequencies would require a reduction in these path lengths through a small-scale photonic integrated circuit. The clock frequency is also limited by rise and fall times of the RT-SOA as well as by the nonlinear gain recovery within the TW-SOA.

The generation of the clock signal in our experiment starts once the input power is raised above the upward switching threshold; we commonly used the polarization controller in front of the FP-SOA for this purpose. Future research will focus on controlling the phase of the clock signal using an auxiliary optical signal.

V. Conclusion

All-optical square-wave generation has been demonstrated using an all-optical flip-flop, created using a bistable RT-SOA and a TW-SOA. Clock operation is wavelength tunable (shown here for several cases near 1590 nm), of variable clock frequency, and requires only dc-driven active components. Optical clocks demonstrated in this letter may find applications in photonic integrated circuits for providing timing and control signals. The techniques used here may also be applicable to all-optical flip-flops made using other waveguide and free-space geometries. Future work will explore dynamic all-optical control of clock phase, increasing the clock frequency, and integration of devices.

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